ABSTRACT OF THE DISCLOSURE

Described are high-speed differential flip-flops. A flip-flop in accordance with one embodiment incorporates some combinational logic, eliminating the need for separate combinational logic when the flip-flop is employed in certain circuit configurations. A flip-flop in accordance with another embodiment includes differential input and output stages, each of which includes a transistor connected across its differential output terminals. The transistors are clocked to short the differential output terminals between expressions of logic levels, thereby limiting the maximum amount of voltage swing required to express subsequent logic levels.